

**REMARKS**

The amendment to the claims is supported by the disclosure at page 15, line 29 to page 16, line 1 and by Figures 2f, 3, 4 and 5 which show a via 64 above the antifuse layer 204 which defines the location of at least one antifuse (where the antifuse layer has not been removed). Applicants submit that the amendment does not add any new matter to the disclosure.

The invention centers on novel interconnect structures having an anti-fuse formed as a layer having openings that define via locations. The structures of the invention advantageously incorporate anti-fuses at reduced manufacturing cost.

Huang (US 6156648) discloses a dual damascene process where interconnection between different metal levels is formed through a patterned dielectric layer. No antifuses are formed in the structures or process of Huang. The cap layer 204 of Huang acts as a diffusion barrier. Cap layer 204 is not retained under any of the vias so as to form an antifuse on filling of the vias. Thus, applicants submit that Huang does not disclose or suggest an antifuse layer which defines interconnect via locations and is also an antifuse.

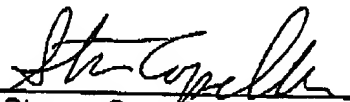
Go et al. (US 5592016) discloses anti-fuse structures which are located above or below vias. Go et al. does not disclose or suggest or suggest an antifuse layer which defines interconnect via locations and is also an antifuse. Applicants submit that the combination of Go et al. with Huang would only result in conventional antifuses of Go et al. being formed in combination with damascene interconnect structures.

Shroff et al. (US 6515343) discloses various antifuse structures and materials. Shroff et al. does not disclose or suggest or suggest an antifuse layer which defines interconnect via locations and is also an antifuse. Applicants submit that the combination of Shroff et al. with Huang would only result in conventional antifuses of Shroff et al. being formed in combination with damascene interconnect structures.

Dixit et al. (US 5233217) discloses conventional anti-fuse structures where the antifuse material is deposited into formed vias. Dixit et al. does not disclose or suggest or suggest an antifuse layer which defines interconnect via locations and is also an antifuse. Applicants submit that the combination of Dixit et al. with Huang would only result in conventional antifuses of Dixit et al. being formed in combination with damascene interconnect structures.

For the above reasons, applicants submit that the claims as amended are patentable over the prior art of record and that the application is in condition for allowance. Such allowance is earnestly and respectfully solicited.

Respectfully submitted,  
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